that an oxide layer is an insulating layer whereas an active area is a conductive area." The applicant respectfully submits that "active area" is known to have a broader definition than just "a conductive area."

Li, identified above, is drawn to a read only memory array and uses the terms "active area" and "active region" in a manner known to those skilled in the art. The term "active area is defined by the following sentence:

> "This array 5 is defined within a single piece of active area of silicon, which is isolated from other active areas by areas of field oxide." Column 5, lines 34-36.

According to Li the term "active area" refers to everything in a semiconductor device that lies between areas of field oxide. "Active area" and "active region" are used interchangeably and both are used to refer to two different aspects of the semiconductor device between areas of field oxide.

"Active region" is often used to refer to a three-dimensional volume of a silicon substrate in which conduction may take place. This is the meaning referred to by the Examiner in stating that "an active area is a conductive area." Final Office Action, Paragraph 17. Li refers to this meaning in the following statement: "A compact ROM array is formed in a single active region (5)," Abstract. This meaning is also referred to in Hikawa, identified above, which defines "active region" as a channel 24 shown in Figure 2, a channel 54 shown in Figure 21, and a channel 74 shown in Figure 26. The channels 24, 54, and 74 are three-dimensional regions of a substrate under gate oxide, and between isolating regions or source and drain regions.

The term "active area" clearly includes more than just the three-dimensional volume of conductive substrate described above, but everything in between the areas of field oxide, including gate oxide and features on the gate oxide. This is expressed in Li in the following clauses:

> "In each of the above two cases, therefore, large amounts of field oxide isolation are required to produce the ROM block. Such areas of field oxide isolation are undesireable because the process of growing field oxide layers causes the field oxide to eat into the active areas thereby reducing their size." Column 2, lines 27-32.

> "This array 5 is defined within a single piece of active area of silicon, which is isolated from other active areas by areas of field oxide." Column 5, lines 34-36.
>
> "Well-known photolithography and etch techniques are used to define the active region with photoresist 200 and to remove the silicon nitride at the areas where field oxide is to be grown. Since there is no field oxide within the ROM array, the active region is a single piece of area with the field oxide surrounding it." Column 7, lines 9-16.
>
> "Since the active area is large, wafer cleaning before gate oxide growth is desirable to avoid defects." Column 7, lines 31-32.

It is clear that the "active area" referred to above must include the silicon substrate, the gate oxide, and features above the gate oxide that all lie between areas of field oxide. "Active area" is used in the sentence about cleaning the wafer to avoid defects in the gate oxide, indicating that the gate oxide is part of the "active area." The background indicates that a growing field oxide eats into active areas that include both a silicon substrate and gate oxide. Also, the ROM array needs a layer of gate oxide and features above it to operate. If "active area" were limited to the definition of the Examiner, the gate oxide and everything above it would be excluded, and this would be inconsistent with the use of "active area" in Li as including the ROM array.

Looking at Figures 2-10 of Li, the field oxide 170 is shown as a thick layer of oxide with a bird's beak shape that can be produced by the known LOCOS process of growing field oxide. In all of the Figures 2-10 a thin layer of oxide extends across the entire active area between the areas of field oxide 170. In Figure 2 a pad oxide 130 covers the substrate 160. In Figures 3 and 4 sacrificial oxide 131 stretches between the areas of field oxide 170 during processing steps. A gate oxide 150 is grown in Figure 5 covering the entire substrate 160 between the areas of field oxide 170, and remains through Figures 6-10. The gate oxide 150 is coextensive with the active area as described by Li, being "isolated from other active areas by areas of field oxide." Column 5, lines 36-37. Therefore, in all of the Figures 5-10 of Li there is a gate oxide 150 that is the only feature that is everywhere the "active area" of Li is.

Li thereby indicates the meaning of the terms "active area" and "active region" as is known to those skilled in the art.

Looking now at Figures 2A-2D of the application, one skilled in the art will recognize the similarity between the layer 215, which the applicant calls the active area 215 in the original

description, and the gate oxide 150 in Figures 5-10 of Li. One skilled in the art will also recognize the similarity between the birds beak shapes in Figures 2A-2D and the birds beak shape of the field oxide 170 of Figures 5-10 of Li. Looking at Li and Figures 2A-2D, one skilled in the art would understand that the described active area 215 is a layer of oxide 215 that is coextensive with the active area 215 in Figures 2A-2D and is isolated from other active areas by birds beak shaped field oxide. One skilled in the art would come to this conclusion based on the knowledge of the art as represented by Li, and from all the other evidence in the application including:

1. The deposition characteristics illustrated in Figure 1 showing a difference in incubation time for deposition of spacer materials on oxide versus another material.
2. The description and illustration in Figure 2B that the spacer 210 is deposited to less than its incubation thickness on oxide, and therefore accumulates only the electrode 205 and not on the active area 215.
3. The selections from the textbooks of Neil H. E. Weste & Kamran Eshraghian and Lance A. Glasser & Daniel W. Dobberpuhl.
4. The recitation of an insulating layer in the original claims 9 and 11.
5. The fact that a CMOS device includes gate oxide between a substrate and a gate electrode.

Reply to the Examiner's Response to Arguments

The Examiner drafted a response to the arguments presented by the applicant in the response filed on December 28, 1999, and the applicant respectfully requests reconsideration in view of the following remarks made in reply. The remarks are organized and identified according to the paragraph numbers used by the Examiner.

Reply to Paragraph 11

The Examiner stated that "the drawings do not illustrate layer 215 as being an oxide layer." The applicant respectfully submits that one skilled in the art, looking at Figures 1 and 2A-2D, and reading the specification, would understand that the layer 215 in the drawings does, in fact, illustrate oxide. This is reinforced by the known meaning of the term "active area" as

demonstrated above. Under *Vas-Cath* and *In re Heinle* the applicant's amendment to the specification is therefore not new matter.

Reply to Paragraph 12

The Examiner stated that the applicant said that an active area mask comprises an active area and an insulating area. This is not a statement that the applicant made. In referring to selections from the textbooks of Neil H. E. Weste & Kamran Eshraghian and Lance A. Glasser & Daniel W. Dobberpuhl, the applicant was establishing the known meaning of the term "active area." The meaning is given in a quote from one of the texts: "oxide thickness is the primary parameter used to distinguish active (transistor) areas from inactive (field) areas." One skilled in the art therefore understands that oxide is an essential and defining part of an active area.

Reply to Paragraph 13

The Examiner indicated that the invention is not described in the specification in such a way as to enable one skilled in the art to make and/or use the invention. The applicant respectfully traverses. The disclosure is available in its entirety to one skilled in the art to determine how to make and use the invention. There is a clear connection in the description between Figures 1 and 2A-2D. The description specifically states that "Figures 2A-2D show how this incubation time difference 130 [illustrated in Figure 1] can be exploited for selective spacer deposition." Specification page 4, lines 19-20.

The Examiner is suggesting that the spacer 210 could have been formed by another method not described in the specification. While thay may be possible, it is irrelevant to the issue of what one skilled in the art would understand upon reading the description and Figures, which is that the layer 215 is an oxide layer 215.

Reply to Paragraph 14

The Examiner stated that the applicant argued that the thickness of the oxide layer 215 defines what is the active area. The applicant did not make this statement. What the applicant said was that, given the meaning of "active area" derived from the selections from the textbooks of Neil H. E. Weste & Kamran Eshraghian and Lance A. Glasser & Daniel W. Dobberpuhl, it is

not incorrect to point to a layer of oxide and call it an active area, as the applicant has done in the original specification. One skilled in the art understands that oxide is an essential and defining part of an active area.

The Examiner stated that there is no support in the specification for an active area layer 215 comprising two separate layers. This is not a statement made by the applicant.

Reply to Paragraph 15

The applicant respectfully submits that the word "reoxidation" implies to one skilled in the art the existence of an original layer of oxide, the oxide layer 215.

Reply to Paragraph 16

The applicant respectfully submits that the "insulating layer" recited in the original claims 9 and 11 provides additional support for the amendment including the term "oxide layer 215." The claims are part of the original disclosure, and provide further indication that the amendment does not include new matter.

Reply to Paragraph 17

The applicant respectfully submits that one skilled in the art reading the application has a working knowledge of CMOS devices, and that a CMOS device has a layer of gate oxide between a substrate and an electrode. Therefore, in contemplating the nature of CMOS devices, the descripion, and the figures, one skilled in the art would understand that the layer 215 is oxide, and the amendment including the term "oxide layer 215" does not contain new matter.

The Examiner stated that "an artisan can not hypothesize the construction and usage of a claimed invention." However, one skilled in the art would not have to hypothesize about the construction and usage of the claimed invention. Furthermore, this is an incorrect statement of the relevant inquiry as set out in *Vas-Cath*:

> "A fairly uniform standard for determining compliance with the "written description" requirement has been maintained throughout: "Although [the applicant] does not have to describe exactly the subject matter claimed,.....the description must clearly allow persons of ordinary skill in the art to recognize that [he or she] invented what is claimed." *Vas-*

Cath, 19 USPQ2d at 1116.

The issue is what one skilled in the art would understand upon combining what is known in the art with the description and the figures. The applicant has demonstrated that one skilled in the art would clearly recognize that the applicant invented what is claimed.

The applicant demonstrated above that the term "active area" known to those skilled in the art includes anything inside the borders of field oxide, including substrate, gate oxide, and features thereon.

Reply to Paragraph 18

In the office action dated October 14, 1999, the Examiner rejected claims under 35 USC § 103(a) based on a combination of references. The applicant traversed the rejection by first pointing out why each reference did not show at least one of the features of the claimed invention. This is a valid response to a rejection under 35 USC § 103(a) because the combined references must show all the elements recited in the claims. If there is an element recited in the claims that is not disclosed in any of the references, then the claims cannot be rejected in view of the combination. In this application, none of the applied references show the spacer comprising silicon nitride or an amorphous silicon film that is not in contact with the oxide layer as recited in claim 23.

Reply to Paragraph 19

Dembiczak requires that a clear and particular teaching or motivation to combine references must be found in the references themselves to support a rejection under 35 USC § 103(a). Without such a clear and particular teaching the combination does not render the claimed invention obvious. The Examiner has combined four references, Ho, Keller, Manning, and McLevige, to reject several of the pending claims, but has not identified text or evidence suggesting the combination of all four references. The Examiner has combined Ho, Keller, Manning, McLevige, and Gonzalez to reject others of the claims, and has not identified text or evidence suggesting the combination of all five references. A general allegation that the combination would produce a "better" result is not a clear and particular showing, and relies

improperly on hindsight.

CONCLUSION

The applicant respectfully submits that all of the pending claims are in condition for allowance and such action is earnestly solicited. The Examiner is invited to telephone the below-signed attorney at 612-373-6973 to discuss any questions which may remain with respect to the present application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

KLAUS FLORIAN SCHUEGRAF ET AL.

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Date 25 APR 2000 By _____
Robert E. Mates
Reg. No. 35,271

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Box AF, Assistant Commissioner of Patents, Washington, D.C. 20231 on April 25, 2000

Tina Pugh
Name

_____
Signature